CERTIFICATE OF TRANSLATION

I, SHUSAKU YAMAMOTO, patent attorney of Fifteenth Floor, Crystal Tower, 1-2-27 Shiromi, Chuo-ku, Osaka 540-6015, Japan HEREBY CERTIFY that I am acquainted with the English and Japanese languages and that the attached English translation is a true English translation of what it purports to be, a translation of Japanese Laid-open Publication No. 60-32565, entitled "Power Source Circuit", laid-opened on February 19, 1985.

Additionally, I verify under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 11th day of June, 1998.

Shusaku Yamamoto

SHUSAKU YAMAMOTO

Your Ref: 02445.037

Translation of Japanese Laid-Open Publication

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Application Number: 58-139639
Filing Date: July 30, 1983
Inventor: J. TAKERA
Applicant: MATSUSHITA ELECTRIC WORKS LTD.

1. TITLE OF THE INVENTION

POWER SOURCE CIRCUIT

2. CLAIM

(1) A power source circuit comprising: a first capacitor to be charged with a voltage obtained by rectifying and smoothing a voltage of an AC power source; a second capacitor connected to the first capacitor via a switching element and an inductance element; and a switch control circuit for turning OFF the switching element when a charging voltage of the second capacitor reaches a prescribed upper limit voltage value and for turning ON the switching element when the charging voltage reaches a prescribed lower limit voltage value.

3. DETAILED DESCRIPTION OF THE INVENTION

[Field of the Invention]

The present invention relates to a power source circuit for obtaining a DC power for a control circuit such as a sequencer from a commercial power source.

[Prior Art]

Conventionally, a power source circuit of this type obtains a DC voltage from the voltage of the commer-

cial power source of AC 100 V. In this case, the input voltage has been set so as to be variable within an allowable range of about -15% to about +10%. However, in general, a control circuit such as a sequencer is not only supplied to meet a domestic demand, but also exported to various foreign countries. Thus, in order to adapt such a control circuit to be compatible with foreign power sources of 110 V, 120 V, 220 V and the like, the components used must be replaced and various tests must be performed as necessitated. Since such tasks are troublesome, it has been desired to solve this problem.

[Objective of the Invention]

In view of the above-described respects, the present invention has been devised for the purpose of providing a power source circuit which can enlarge the allowable varying range of an input voltage from the commercial power source, can obtain a DC low voltage with a minimum loss, and is configured so as to be accommodated to not only domestic demands but also overseas demands.

[Disclosure of the Invention]

Hereinafter, the configuration according to the present invention will be described by way of an example illustrated in the drawings. Figure 1 is a circuit diagram showing the entire configuration of the power source circuit in an example of the present invention, and Figure 2 is a circuit diagram of the principal section thereof. As shown in Figure 1, the AC input voltage from a commercial power source 1 is reduced by a power transformer 2, full-wave rectified by a diode bridge 3 and then

charged in a capacitor C_0. The charging voltage of the capacitor C_0 is charged into a capacitor C_1 via a switching element 6 (the ON/OFF states of which are controlled by a switch control circuit section 4) and an inductance element L. The charging voltage V_R (= 8 V) of the capacitor C_1 is used as power for driving the relays in a sequencer. A three-terminal regulator 6 generates a power source voltage Vcc (= 5V) for driving the sequencer IC as a charging voltage of a capacitor C_2 (the charging voltage of the capacitor C_1 is assumed to be a constant voltage). This three-terminal regulator is a series regulator generally used as a constant voltage circuit. Such a regulator is widely available as an IC package. Figure 2 is a circuit diagram showing the configuration of a switching type pre-regulator. In the circuit shown in Figure 2, a transistor Tr_1 is used as the switching element 5. The switch control circuit 4 is implemented as a hysteresis circuit including a comparator 7. The charging voltage of the capacitor C_0 is applied to a Zener diode Z via a current-limiting resistor. The cathode of the Zener diode Z is connected to the positive input terminal of the comparator 7 via a resistor r. The positive input terminal of the comparator 7 is also connected to the output terminal of the comparator 7 via another resistor r. Thus, the voltage applied to the positive input terminal of the comparator 7 equals a voltage obtained by dividing a voltage difference between a reference voltage generated on the cathode of the Zener diode Z and the output voltage of the comparator 7 by a pair of resistors r. A voltage obtained by dividing the charging voltage of the capacitor C_1 by the resistors R_1 and

R_2 is applied to the negative input terminal of the comparator 7. The operating voltage of the comparator 7 is supplied from the capacitor C_0. When the output of the comparator 7 reaches the H level, a transistor Tr_2 is turned ON and the transistor Tr_1 is also turned ON via base current flowing through a resistor r_b. On the other hand, when the output of the comparator 7 reaches the L level, the transistor Tr_2 is turned OFF and the transistor Tr_1 is also turned OFF. It is noted that when the output of the comparator 7 is at the H level, the upper limit value of the voltage thereof is limited to the base-emitter voltage V_{BE} (= 0.7 V) of the transistor Tr_2. The pre-regulator circuit shown in Figure 2 has a very simple circuit configuration utilizing the hysteresis characteristics of the comparator 7. That is to say, the feature of the circuit according to the present invention lies in setting a ripple voltage and circuit constants, unlike a conventional variable frequency or constant frequency switching regulator having a variable duty ratio.

Hereinafter, the operation of this circuit will be described with reference to Figure 3. Figure 3(a) shows the variation of the charging voltage V_R of the capacitor C_1. In Figure 3(a), V_{rp} denotes a ripple voltage and V_{RH} and V_{RL} denote the upper limit value and the lower limit value of the charging voltage V_R of the capacitor C_1, respectively. Figure 3(b) shows the variations of the voltage applied to the positive input terminal of the comparator 7, in which Vh denotes the higher applied voltage and Vl denotes the lower applied voltage. In the circuit shown in Figure 2, in the period after the power is

supplied and until the voltage V_R reaches the voltage V_{RH} shown in Figure 3, the transistor Tr_1 is conductive (i.e., in the ON state). When the voltage V_R reaches the voltage V_{RH}, the output of the comparator 7 becomes low, so that the transistor Tr_2 is turned OFF and the transistor Tr_1 is also turned OFF. While the transistor Tr_1 is OFF, power is supplied from the capacitor C_1 to a load. Thus, the charge in the capacitor C_1 is discharged and the voltage V_R becomes low. At this time, the voltage Vl is being applied to the positive input terminal of the comparator 7. When the charging voltage V_R of the comparator 7 reaches the voltage V_{RL}, the capacitor 7 is turned OFF, the transistor Tr_2 is turned ON and the transistor Tr_1 is also turned ON. As a result, the capacitor C_1 is charged again from the capacitor C_0. At this time, the voltage Vh is being applied to the positive input terminal of the comparator 7. Thereafter, when the charging voltage V_R of the capacitor C_0 reaches the voltage V_{RH}, the transistor Tr_1 is turned OFF again. In this way, every time the voltage V_R reaches the voltage V_{RH} or V_{RL}, the transistor Tr_1 is turned ON/OFF, as shown in the waveform chart in Figure 3.

Hereinafter, a method for setting the respective constants of the circuit shown in Figure 2 will be described. First, V_{RL} is set so as to satisfy the following equation.

$$\frac{R_2}{R_1 + R_2} V_{RL} = \frac{V_Z - V_{CE}}{2r} \cdot r + V_{CE} \doteqdot \frac{V_Z}{2}$$

where V_{CE} is an output voltage at the open collector of the comparator 7 and is approximately equal to zero, and V_Z is

a Zener voltage of the Zener diode Z. The voltages Vl and Vh are given by the following equations.

$$V\ell = \frac{Vz - V_{CE}}{2r} \cdot r + V_{CE} \fallingdotseq \frac{Vz}{2}$$

$$Vh = \frac{Vz - V_{DE}}{2r} \cdot r + V_{BE}$$

$$\fallingdotseq \frac{Vz - 0.7}{2} + 0.7 = \frac{Vz}{2} + \frac{0.7}{2}$$

where V_{BE} is the base-emitter voltage of the transistor Tr when the output of the comparator 7 is at the H level and is approximately equal to 0.7 V. The ripple voltage Vrp may be calculated based on the following equation.

$$Vrp = V_{RH} - V_{RL} = \frac{R_1 + R_2}{R_2} (Vh - V\ell)$$

Moreover, the constants of the inductance element L and the capacitor C_1 can be determined based on the following equations, where V_D is a charging voltage of the capacitor C_0; t_1 is an ON time period of the transistor Tr_1; t_2 is an OFF time period of the transistor Tr_1; I_P is current flowing through the inductance element L while the transistor Tr_1 is ON; I_0 is a load current; I is an effective current; I_{C1} is a current flowing through the capacitor C_1; and P_2 is the wattage of the load.

$$Ip = \frac{V_D - V_{RL}}{L} \cdot t_1 \quad \cdots\cdots\cdots\cdots \quad (1)$$

$$(Ip - I_0)\, t_1 = C_1 \cdot Vrp \quad \cdots\cdots\cdots\cdots \quad (2)$$

$$\left(\frac{V_D - V_{RL}}{L} t_1 - I_0\right) t_1 = C_1 \cdot Vrp \quad \cdots\cdots \quad (3)$$

$$t_2 = \frac{\frac{1}{2}LI^2 + \frac{1}{2}C_1(Vh^2 - V\ell^2)}{Pz} \fallingdotseq \frac{C_1}{2Pz}(Vh^2 - V\ell^2) \quad \cdots\cdots\cdots\cdots \quad (4)$$

$$I = Ip\frac{t_1}{t_1 + t_2} \quad \cdots\cdots\cdots\cdots \quad (5)$$

$$I = I_0 + Ic_1$$

Based on equations (1) and (2) among the above equations, the ON time period t_1 of the transistor Tr_1 can be calculated. The load current I_0 is determined in accordance with the wattage P_z of the load. In this case, since the voltage V_D is a rectified and smoothed output of the transformer 2, a voltage V_D corresponding to the maximum value of the input voltage is determined and then the duty ratio at this voltage is set at 1/2. That is to say, the load current I_P is calculated from equations (2) through (4) under the condition $t_1 = t_2$. Moreover, the value of L is set based on equation (1), and t_1 is obtained from equation (1). The value of C_1 is set based on equation (2). Furthermore, by setting $I_{max} = I_P \cdot 1/2$ based on equation (5), the current capacitance of the transistor Tr_1 and the inductance element L is obtained. In the power source circuit having the above-described configuration, the operation can be guaranteed at input voltages ranging from about AC 85 V to about 150 V. Thus, the power source circuit of the present invention can meet both domestic demands and overseas demands that require different power source voltages.

[Effect of the Invention]

The power source circuit of the present invention

has the above-described configuration and includes: a first capacitor to be charged with a voltage obtained by rectifying and smoothing a voltage of an AC power source;
a second capacitor connected to the first capacitor via a switching element and an inductance element; and a switch control circuit for turning OFF the switching element when a charging voltage of the second capacitor reaches a prescribed upper limit voltage value and for turning ON the switching element when the charging voltage reaches a prescribed lower limit voltage value. Thus, even when the charging voltage of the first capacitor greatly varies because of large variations of the commercial power source voltage in a wide range, the charging voltage of the second capacitor varies between the prescribed upper and lower limit voltage values which have been determined by the switch control circuit. Thus, the power source circuit of the present invention can be used in a wide voltage range and can advantageously meet both domestic demands and overseas demands requiring different power source voltages. Furthermore, according to the present invention, since the current limiting element serially connected to the switching element is an inductance element, the loss caused during the current limitation can be reduced to a low level, and the amount of generated heat can also be advantageously reduced.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram showing an example of the power source circuit according to the present invention; Figure 2 is a circuit diagram showing the principal section thereof; and Figure 3 is a diagram

illustrating the operation thereof.

1: commercial power source; 2: voltage step down transformer; 3: diode bridge; 4: switch control circuit; 6: switching element; L: inductance element; and C_1 and C_2: capacitors.

また本発明においてはスイッチング素子と直列接続された限流要素はインダクタンス素子であるので、限流時に生じる損失も小さく抑えることができ、発熱量も少なくすることができるという利点もある。

4.図面の簡単な説明

第1図は本発明の一実施例の回路図、第2図は同上の要部回路図、第3図は同上の動作説明図である。

(1)は商用電源、(2)は降圧トランス、(3)はダイオードブリッジ、(4)はスイッチコントロール回路、(5)はスイッチング素子、Lはインダクタンス素子、C_1,C_2はコンデンサである。

代理人 弁理士 石田長七

FIG. 1

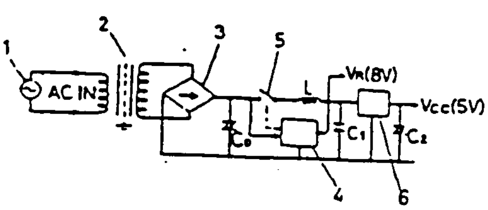


FIG. 2

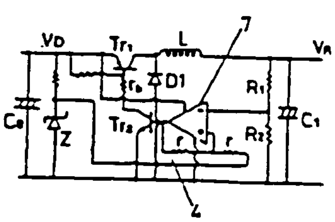
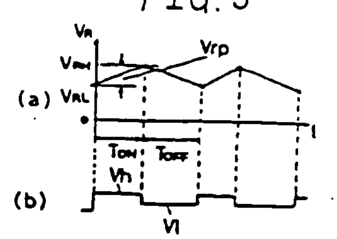


FIG. 3



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㊴発明の名称　電源回路

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⑫発 明 者　武良　丈治　門真市大字門真1048番地　松下電工株式会社内

⑪出 願 人　松下電工株式会社　門真市大字門真1048番地

⑭代 理 人　弁理士　石田　長七

明　細　書

1. 発明の名称

電源回路

2. 特許請求の範囲

(1) 交流電源電圧の整流平滑電圧を充電される第1のコンデンサと、スイッチング素子およびインダクタンス素子を介して第1のコンデンサに接続される第2のコンデンサと、第2のコンデンサの充電電圧が所定の上限電圧値に達したときにスイッチング素子をオフし、前記充電電圧が所定の下限電圧値に達したときにスイッチング素子をオンするスイッチコントロール回路とを有して成ることを特徴とする電源回路。

3. 発明の詳細な説明

〔技術分野〕

本発明はシーケンサのような制御回路の直流電源を商用電源から取り出す電源回路に関するものである。

〔背景技術〕

従来、この種の電源回路はAC100Vの商用電源電圧から直流電圧を得るようにしていた。そしてこの場合、入力電圧としては－15%～+10%程度の電圧変動が許容範囲として設定されていた。しかしながら、一般にシーケンサのような制御回路は、国内の需要に供されるのみならず、外国に輸出されることも多く、110V，120V，220V等の国外向電源仕様のものについては使用部品を変更したり、それに伴う種々の試験等を行なう必要があつて、業務上煩しさが多く、その解決が望まれていた。

〔発明の目的〕

本発明は上述のような点に鑑みて為されたものであり、商用電源からの入力電圧の変動許容範囲を広くして、しかも仕向先で直流出力電圧を得ることができ、国内向の需要にも国外向の需要にも対応できるようにした電源回路を提供することを目的とするものである。

〔発明の開示〕

以下本発明の構成を図示実施例について説明す

フ、オンを繰り返す。

以下、第2図の回路における各定数の設定方法について述べる。まず、V_{RL}は次式によつて設定される。

$$\frac{R_2}{R_1+R_2}V_{RL}=\frac{V_Z-V_{CE}}{2r}\cdot r+V_{CE}\fallingdotseq\frac{V_Z}{2}$$

ただし、上式においてV_{CE}はコンパレータ(7)のオープンコレクタ出力電圧であつて、ほぼ0である。またV_ZはツエナダイオードZのツエナ電圧である。また、電圧V_ℓ, V_hは次式によつて設定される。

$$V_\ell=\frac{V_Z-V_{CE}}{2r}\cdot r+V_{CE}\fallingdotseq\frac{V_Z}{2}$$

$$V_h=\frac{V_Z-V_{BE}}{2r}\cdot r+V_{BE}$$

$$\fallingdotseq\frac{V_Z-0.7}{2}+0.7=\frac{V_Z}{2}+\frac{0.7}{2}$$

ただし、V_{BE}はコンパレータ(7)の出力がHレベルの場合におけるトランジスタTrのベースエミツタ間電圧であり、ほぼ0.7Vである。また、リツプル電圧V_{rp}は次式によつて算出できる。

$$V_{rp}=V_{RH}-V_{RL}=\frac{R_1+R_2}{R_2}(V_h-V_\ell)$$

さらにインダクタンス素子LおよびコンデンサC₁の定数は次式によつて決定される。ただし、V_DはコンデンサC_0の充電電圧、t_1はトランジスタTr_1のオン時間、t_2はトランジスタTr_1のオフ時間、I_pはトランジスタTr_1のオン時にインダクタンス素子Lに流れる電流、I_0は負荷電流、Iは平均電流、I_{C1}はコンデンサC_1に流れる電流、P_Zは負荷のワット数である。

$$I_p=\frac{V_D-V_{RL}}{L}\cdot t_1 \quad \cdots\cdots ①$$

$$(I_p-I_0)\,t_2=C_1\cdot V_{rp} \quad \cdots\cdots ②$$

$$\left(\frac{V_D-V_{RL}}{L}t_1-I_0\right)t_2=C_1\cdot V_{rp} \quad \cdots\cdots ③$$

$$t_2=\frac{\frac{1}{2}LI^2+\frac{1}{2}C_1(V_h^2-V_\ell^2)}{P_Z}$$

$$\fallingdotseq\frac{C_1}{2P_Z}(V_h^2-V_\ell^2) \quad \cdots\cdots ④$$

$$I=I_p\frac{t_1}{t_1+t_2} \quad \cdots\cdots ⑤$$

$$I=I_0+I_{C1}$$

上式のうち、①式と③式よりトランジスタTr_1のオン時間t_1が算出できる。負荷電流I_0は負荷のワット数P_Zに応じて定められる。ここで電圧V_Dはトランス(2)の整流平滑出力であるため、入力電圧を最大値に設定したときの電圧V_Dを求めて、このときデューティ比が$\frac{1}{2}$になるように設定する。つまり、$t_1=t_2$として、⑤〜④式により負荷電流I_pを求める。また①式よりLの値を設定し、t_1を求めて、②式よりC_1の値を設定する。さらに⑤式より、$I_{max}=I_p\cdot\frac{1}{2}$としてトランジスタ$Tr_1$およびインダクタンス素子Lの電流容量を求める。以上のようにして構成した電源回路にあつては、入力電圧としてAC 85V〜130V程度の電圧範囲において動作保証が可能であつて、国内向の需要にも、また電源電圧の異なる国外向の需要にも供することができる。

〔発明の効果〕

本発明は叙上のように構成されており、交流電源電圧の整流平滑電圧を充電される第1のコンデンサと、スイッチング素子およびインダクタンス素子を介して第1のコンデンサに接続される第2のコンデンサと、第2のコンデンサの充電電圧が所定の上限電圧値に達したときにスイッチング素子をオフし、前記充電電圧が所定の下限電圧値に達したときにスイッチング素子をオンするスイッチコントロール回路とを有するものであるから、商用電源電圧が広い範囲で変動して第1のコンデンサの充電電圧がかなり大きく変動しても、第2のコンデンサの充電電圧はスイッチコントロール回路によつて設定された所定の上限電圧値と下限電圧値との間で変動することになり、したがつて広い電圧範囲において使用可能となり、国内向の需要にも、また電源電圧の異なる国外向の需要にも供することができるという利点があり、さらに